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A Low power and area efficient CLA adder design using Full swing GDI technique

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Abstract
The low power VLSI design has an important role in designing of many electronic systems. While designing any combinational or sequential circuits, the important parameters like power consumption, implementation area, voltage leakage and performance of the circuit are to be considered. Design of area, high speed and power-efficient data path logic systems forms the largest areas of research in VLSI system design. This paper presents a low power Carry look ahead adder design using Full swing Gate diffusion (FS-GDI) technique. The proposed CLA implementation utilizes improved full-swing GDI F1 and F2 gates, which are the counterparts of standard CMOS NAND and NOR gates. The basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by Full swing GDI technique. The proposed technique utilizes a single swing restoration (SR) transistor to improve the output swing of F1 and F2 GDI gates. A 16-bit CLA is designed and Simulations are performed by Mentor graphics 130nm CMOS technology ELDO simulator. Simulation results have shown a greater reduction in delay, power dissipation and area.

Index Terms: Full swing Gate Diffusion Input (FS-GDI), Low Power Design, Full swing 3T EXOR, delay, efficient area.

I. Introduction

Low power arithmetic circuits have become very prominent these days in VLSI industry. The rapid growth of portable electronics has made the adder circuit as the main building block in DSP processor. Adder is the main component of arithmetic unit. A Complex DSP system involves several adders. CLA is proved to have good performance which is using in high speed adders. High speed, high throughput, small silicon area and low power consumption are the main concerns in designing an efficient adder. Power consumption and area reduction of logic have become primary focuses of attention in VLSI digital design. Power and area directly affects the high performance systems as well as device size and cost. Since the introduction of the standard CMOS Logic in early 80s, many design solutions have been proposed to improve power dissipation, area and performance of digital VLSI chips.

Gate Diffusion Input (GDI) design methodology was introduced as a promising alternative to Static CMOS Logic. Generally it was proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes.GDI methodology allowed implementation of a wide range of complex logic functions by using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library. Recently, it was shown that any GDI circuit can be implemented in a standard CMOS process. Various combinational circuits, such as adders, multipliers, comparators, and counters, were implemented in processes from 0.8 micrometer down to 65 nanometer. But these GDI gates may suffer from threshold voltage drops which reduce current drive and therefore affect the performance of the gate. These drops also increase direct-path static power dissipation in the cascaded inverters, used for swing restoration.

As an alternative Full swing GDI technique came into existence. The adverse effects can be significantly reduced by using swing restoration buffers. This paper presents an efficient methodology for digital circuit's implementation. The proposed methodology was applied to a 16-bit adder in low power standard 130 nm TSMC process. The proposed CLA implementation utilizes improved full-swing GDI F1 and F2 gates, which are the counterparts of standard CMOS NAND and NOR gates. The CLA presents a greater area and power reduction when compared to the conventional CMOS implementation.

II. OVER VIEW OF GDI

The GDI method is based on the use of a simple cell as shown in Fig. 1. The basic cell reminds one of

the standard CMOS inverter, but there are some differences [4].

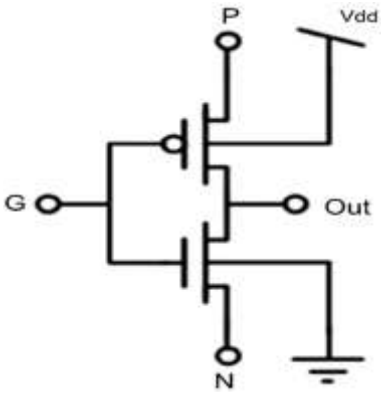


Figure 1: Basic GDI cell

1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).
2) Bulks of both nMOS and pMOS are connected to ground and Vdd (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

Multiple Boolean functions can be implemented by a simple GDI cell, as demonstrated in Table 1. This is achieved by a change of the input configuration of the GDI cell. While implementation of most of these functions is relatively complex (6–12 transistors) in Static CMOS, it is very efficient (only 2 transistors) with the GDI cells. The Multiplexer (MUX) is the most complex function that can be implemented with a basic GDI cell, while being the most efficient function as compared to CMOS implementation.

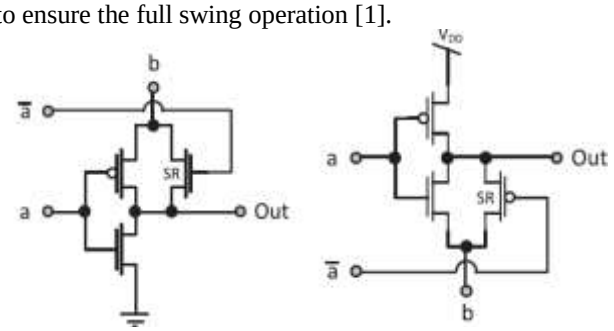
Table 1: Some logic functions that can be implemented with a basic GDI cell.

N	P	G	Output	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

The major drawback of the GDI technique is it suffers from threshold voltage drops which reduce current drive and therefore affect the performance of the gate and increase static power dissipation in the cascaded inverters, used for swing restoration. By using multiple Threshold transistors (Multi V_{TH}) in swing restoration buffer the power dissipation can be reduced. The threshold voltage drops can also be minimized and full swing can be ensured by using swing restoration transistors in the Full swing GDI technique.

III. Full swing gdi

The proposed technique utilizes a single swing restoration (SR) transistor to improve the output swing of F1 and F2 GDI gates .Figure 2 shows the structure of full swing F1 and F2 cells. The SR transistor is activated only in cases when the Vth drop may occur at the output. Since in F1 and F2 gates, the output Vth drop can occur only at one of the logical levels (Vth instead of 0 V in F1, and Vdd–Vth instead of Vdd in F2), only a single SR transistor is required to ensure the full swing operation [1].



a) F1 cell b) F2 cell

Figure 2: FS GDI gates

The gate input signal of GDI cell has an inverted representation in the circuit; it can be used to control the swing restoring transistor. This transistor will have a diffusion input similar to the diffusion input of GDI, but will be of an opposite type (nMOS for F1, and pMOS for F2). In this manner, the diffusion input signal will pass through a pair of transistors of both types (in the transistor of original GDI cell, and the complementary SR transistor). The FS GDI cells are efficient alternative for swing restoration buffers, in designs where inverted signals can be obtained as part of logic function implementation.

IV. PROPOSED 3T EXOR WITH FULL SWING

The Ex-OR gates are the basic building blocks of various digital system applications like adder, comparator, and parity generator/checker and encryption processor. This paper proposes a 3 Transistor Ex-OR circuit which ensures full swing at the output [5]. The new Ex-OR with three transistors is proposed by modifying the existed 3T cross coupled Ex-OR gate to get full output voltage swing**.** This may be an alternative for 6 transistors EXOR gate used for achieving full swing at output in which less number of transistors can minimize the area and power dissipation. The proposed 3T model majorly reduces overall die area and power dissipation of the 16-bit CLA implemented.

The figure 3 shows the proposed 3T EXOR which is implemented in 130nm process technology.

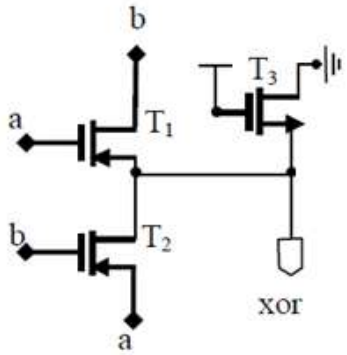


Figure 3: Proposed 3T EXOR with Full swing

Simulation results have shown that the proposed 3 transistor EXOR model ensures Full swing at the output as shown in figure 4.

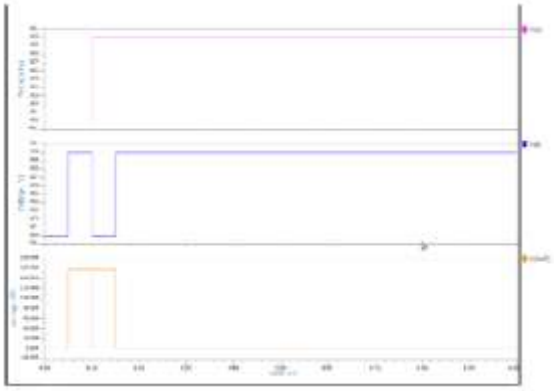


Figure 4: Simulation results of 3T EXOR with Full swing

V. CLA IMPLEMENTATION USING FS GDI

The implementation was based mostly on F1 and F2 cells, assuming the logical functions F1= $\overline{A}B$ and F2= $\overline{A}+B$ The conventional architecture of CLA is shown in figure 5.

The pg unit outputs were implemented as follows [1]

$$p = a \oplus b \quad g = ab$$

The PG unit implementation is the following

$$P = p_1 p_0 \quad G = g_1 + g_0 p_1$$

The local and global carry generator blocks are implemented according to

$$C_{loc} = g_0 + p_0 C_{in} \quad C_{out} = G_1 + P_1 G_0 + P_1 P_0 C_{in}$$

The signals P1, G1 and P0, G0 represent the outputs from top hierarchy level CLA blocks.

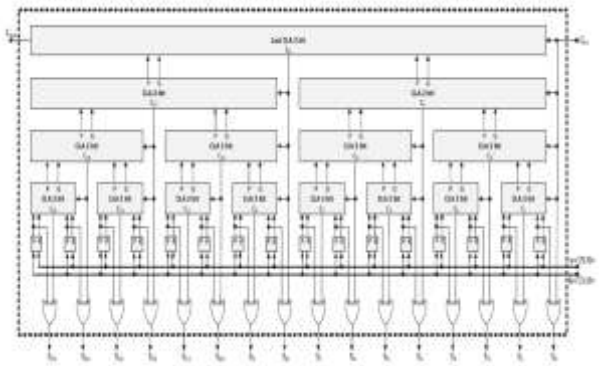


Figure 5: The general CLA architecture

It can be clearly seen that FS GDI implementation have significant advantage in terms of transistors count and area, as compared to CMOS providing full swing and improved performance. It implies about 40% area increase as compared to Multi voltage threshold GDI (MVT GDI)[1]. Still, it occupies only half of area as compared to CMOS design.

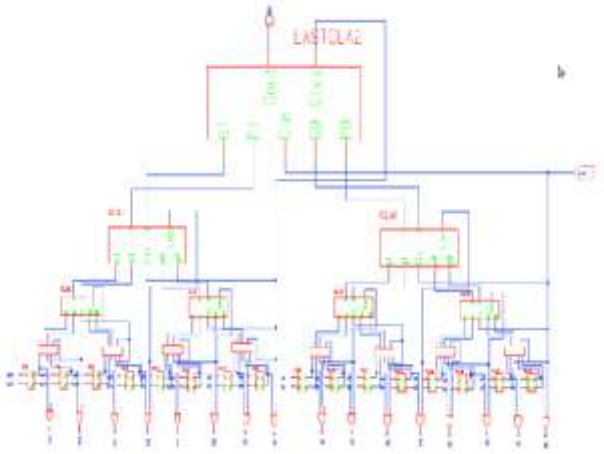
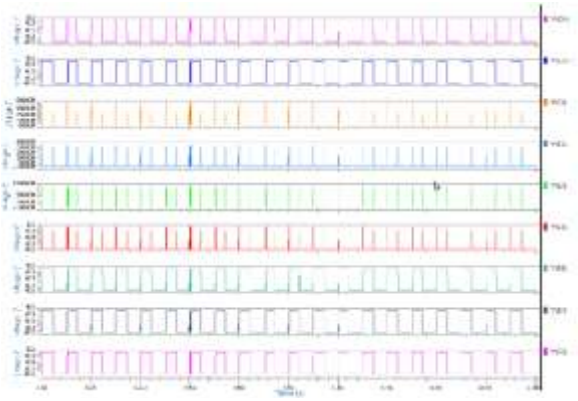


Figure 6: Proposed CLA architecture in 130nm technology

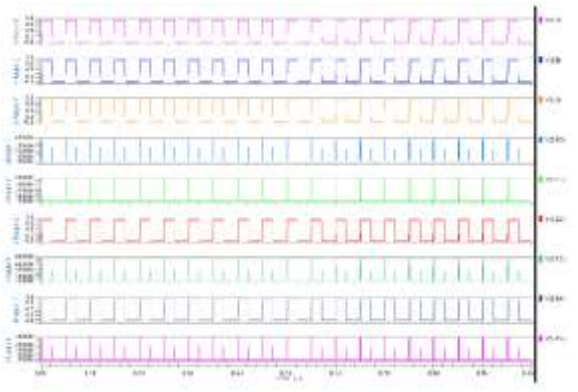
VI. SIMULATION RESULTS AND ANALYSIS

A new CLA adder using full swing GDI technique have been proposed in this paper as shown in figure 6. This adder is evaluated and compared to other GDI adders from the literature. In particular this CLA is implemented using Mentor graphics schematic and layout editor and extracted using 130nm CMOS technology. Simulations are carried out using ELDO, with the capacitances and resistances extracted from the layout. The adder is simulated with 100 MHz frequency and at 27^0C and the supply voltages varying from 0.8 to 1.4V.

The required input pattern- to-input-pattern transitions are included in the test patterns to obtain accurate result. Delay and Power dissipation are measured for the whole 16 bit adder.



a)



b)

Figure 7: Simulation waveforms of 16 bit CLA

It was shown that the overall area and power dissipation has been significantly reduced when compared to other GDI techniques and conventional CMOS technology. The proposed model is compared with the previous models of GDI techniques and the conventional CMOS model.

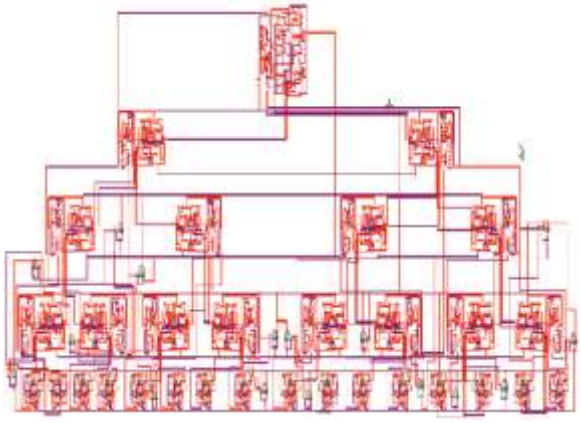


Figure 8: Layout of Proposed 16-bit CLA architecture

An efficient decrease in the transistor count which results in the gradual decrease in the overall area is achieved by the proposed model. The proposed EXOR model with 3 transistors has reduced a total of 48 transistors in the whole circuit reducing the overall die area.

Table 1: Transistor count and area estimation comparison between GDI and Static CMOS designs.

Design	Unit						
	pg	PG	LCG	CLA	Last CLA	EXOR	TOTAL
CMOS	18 (41)	18 (35)	12 (24)	30 (59)	34 (77)	192 (480)	934 (2039)
MVT GDI	8 (12)	8 (12)	8 (12)	16 (24)	24 (36)	64 (93)	438 (657)
FS GDI(6T EXOR)	11 (16)	11 (16)	10 (15)	21 (31)	31 (46)	96 (189)	627 (925)
FS GDI(3T EXOR)	11 (16)	11 (16)	10 (15)	21 (31)	31 (46)	48 (94)	579 (831)

Transistors count (Area [W min L min]).

In general the CMOS design has the shortest delay among all adder implementations. The FS GDI implementation shows a 30% delay increase when compared to CMOS design. Whereas the MVT GDI is about three times slower than CMOS due to voltage drops. The proposed model shows better delay results when compared to the previous GDI techniques. Better performance results can be obtained by the FS GDI model through which the driving capability can be increased by using F1 and F2 cells. The power dissipation has been reduced prominently with the proposed model.

Different types of adders and multipliers can be designed using the FS GDI technique. As an application a Carry skip adder (CSK) and a Carry select adder (CSL) are designed using the full swing GDI technique. Both the adders implemented were of 16 bit. Each and every module of the circuits is designed using the full swing approach.

VII. CARRY SELECT ADDER (USING FS GDI TECHNIQUE)

A 16 bit carry select adder (CSL) is designed using the proposed FS GDI methodology in 130 nm technology. Several internal modules like AND, OR, MUX, HA, FA are designed using the Full swing technique.

The schematic of the proposed 16 bit CSL is shown in figure 9.

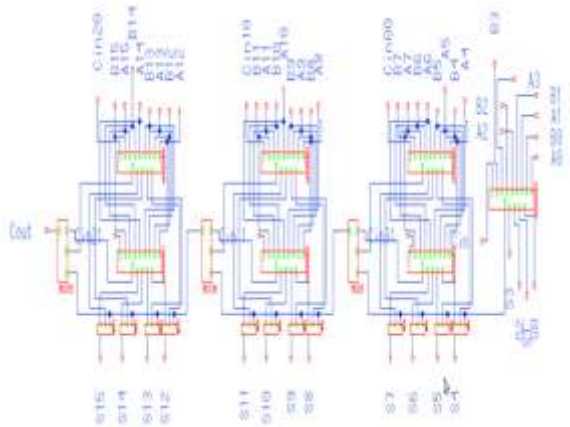
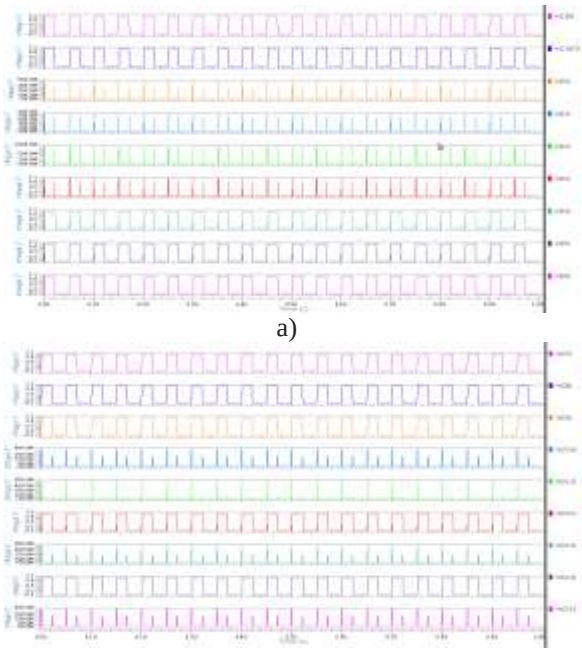


Figure 9: 16 bit CSL (using FS GDI technique)



a)

b)

Figure 10: Simulation waveforms of 16 bit CSL

VIII. CARRY SKIP ADDER (USING FS GDI TECHNIQUE)

A 16 bit carry skip adder (CSK) is designed using the proposed FS GDI methodology in 130 nm technology.

Several internal modules like RCA, OR, 5-INPUT AND are designed using the full swing approach.

The schematic of the proposed 16 bit CSK is shown in figure 11.

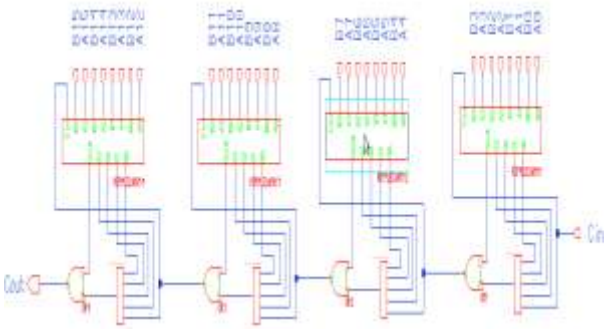
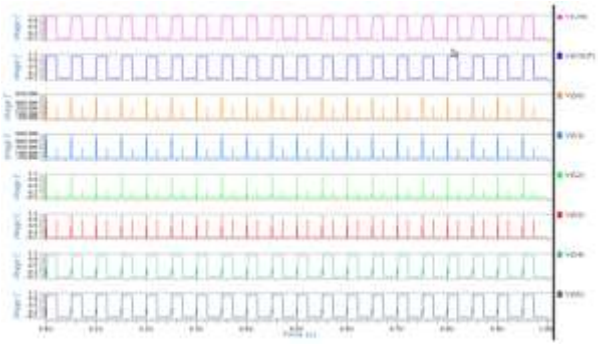
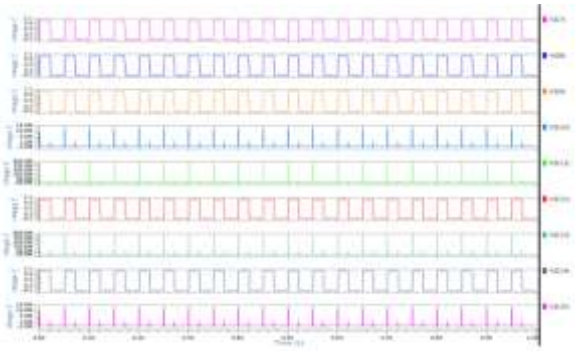


Figure 12: 16 bit CSK (using FS GDI technique)



a)



b)

Figure 13: Simulation waveforms of 16 bit CSK

The delay and power dissipation comparison of the 16 bit CLA and different other adder implementations is shown below

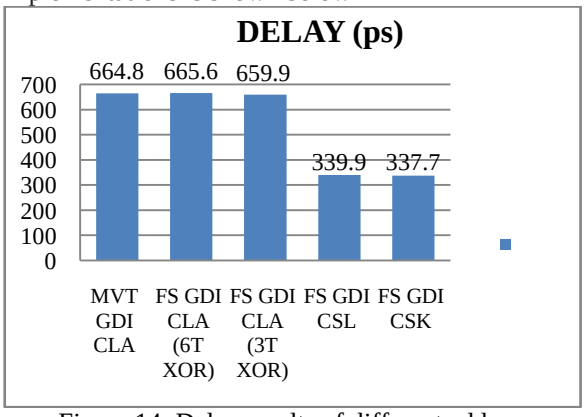


Figure 14: Delay results of different adders

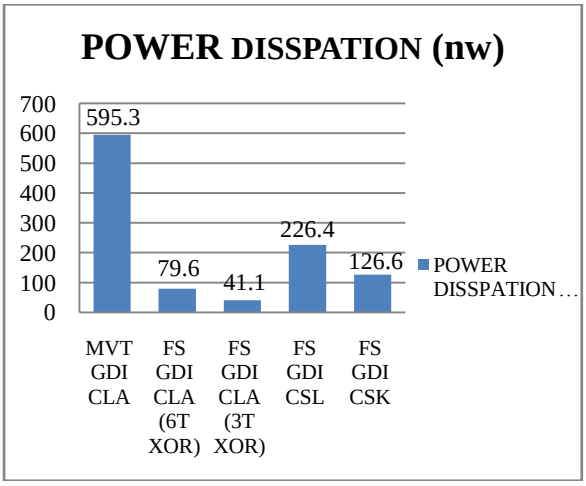


Figure 15: Power dissipation results of different adders

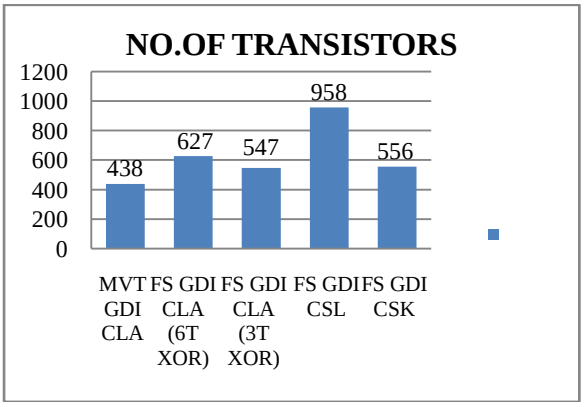


Figure 16: Transistor count of different adders

IX. CONCLUSIONS

In this paper a low power 16 bit CLA adder using full swing GDI technique is proposed. A novel 3Transistor EXOR circuit which produces Full swing at its output is presented. The design and implementation of this CLA using 3T EXOR has shown better results of reduced area and power dissipation. This designed CLA adder circuit successfully operates at low voltages with high driving capability and excellent signal integrity. The adder is operated in low power 130nm CMOS technology and is studied for low power dissipation and reduced area models. Simulations have been carried out using Mentor Graphics ELDO simulator to evaluate the new design. Also different types of adders like Carry select adder and carry skip adder are designed using full swing GDI technique. A wide comparison is made for different designs and a significant improvement in terms of Delay, power dissipation and area parameters are illustrated. A large area reduction and reduction on switching activity is achieved significantly reducing the number of transistors in the circuit. The 16-bit CLA adder using Full swing GDI technique with optimized EXOR circuit produced better delay, reduced power dissipation and area results.

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